

PSEUDO-CODE 100

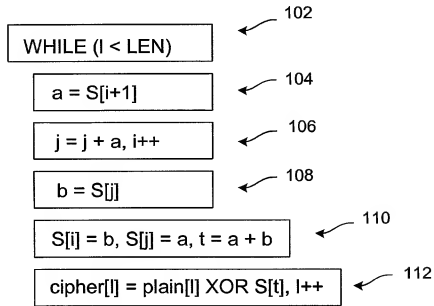
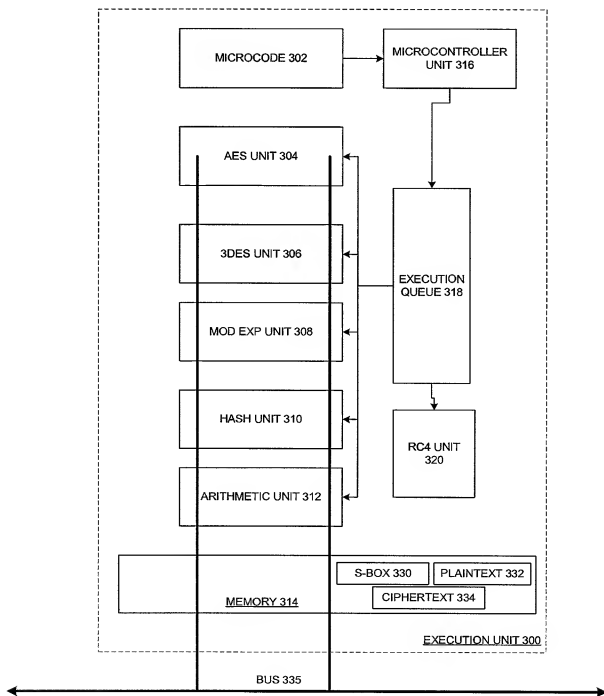


FIG. 1 (PRIOR ART)

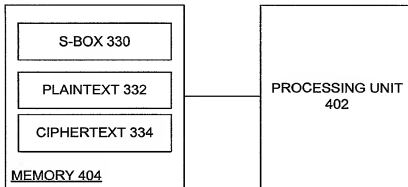
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202	204	206	208	210	212	214	216	218	220	222	224
OPERATION	CYCLE	i	j	a	b	t	i	temp	MEMORY READ (FIRST CYCLE) (MR1)	MEMORY READ (SECOND CYCLE) (MR2)	MEMORY WRITE (MW)
104 → a = S[i+1]	0								S[i]		
106 → i++	1	i + 1								S[i]	
108 → j = j + a	2		j + MR2	MR2							
108 → b = S[j]	3								S[j]		
110 → S[j] = b, t = a + b, temp = plain[j]	4									S[j]	
110 → S[j] = a	5			MR2	MR2 + a				plain[j]		S[j] = MR2
112 → temp = temp XOR S[t]	6								S[t]	plain[j]	S[j] = a
	7 (0)							MR2		S[t]	
	8 (1)							temp XOR MR2			
112 → i++	9 (2)						i + 1				cipher[j] = temp

FIG. 2 (PRIOR ART)

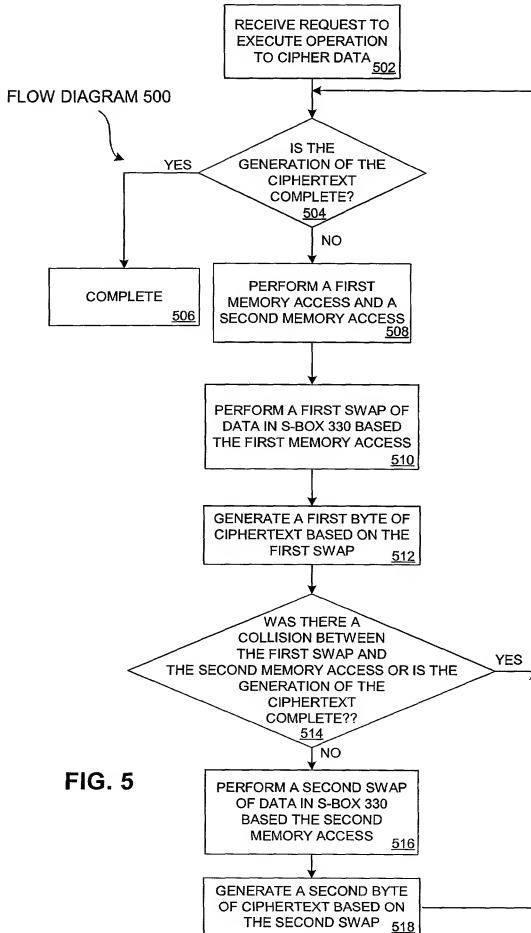


SYSTEM 400



**FIG. 4**

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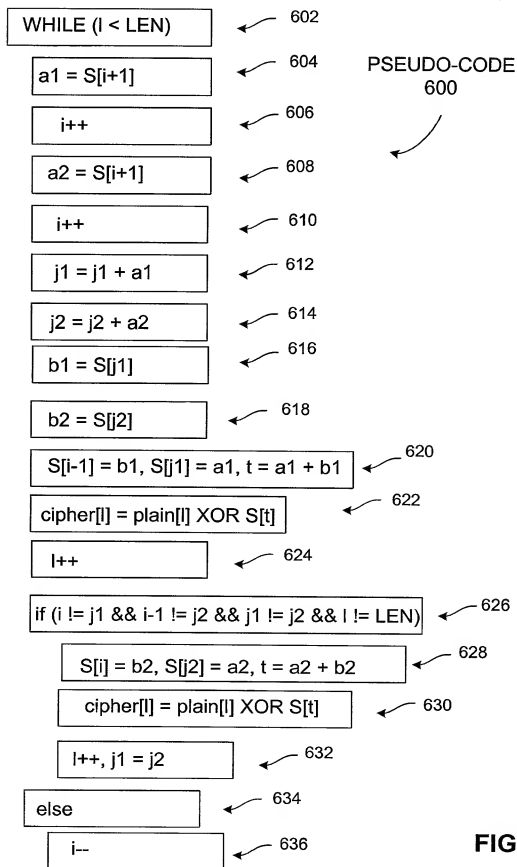


FIG. 6

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[illegible]

**FIG. 7**

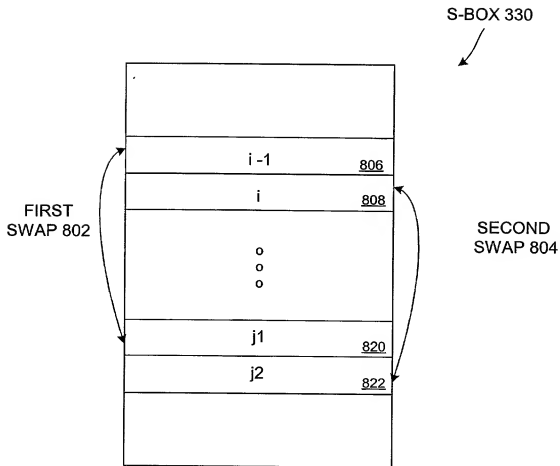


FIG. 8



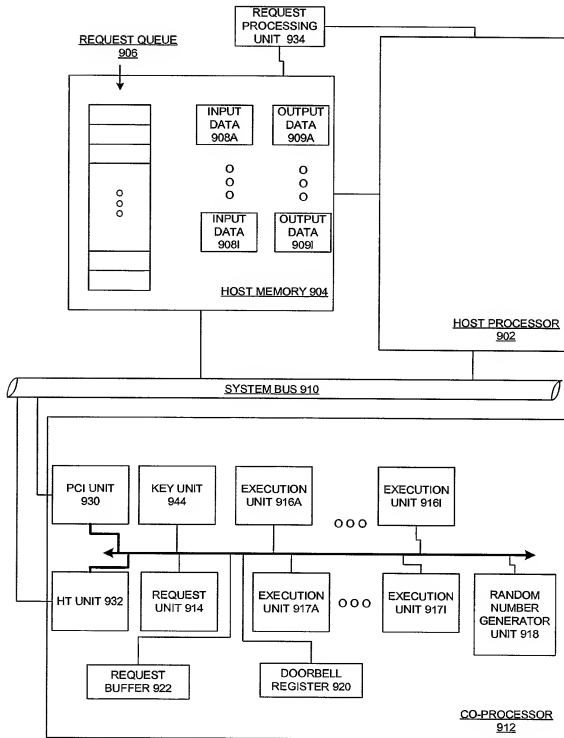


FIG. 9

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